FIG . 1

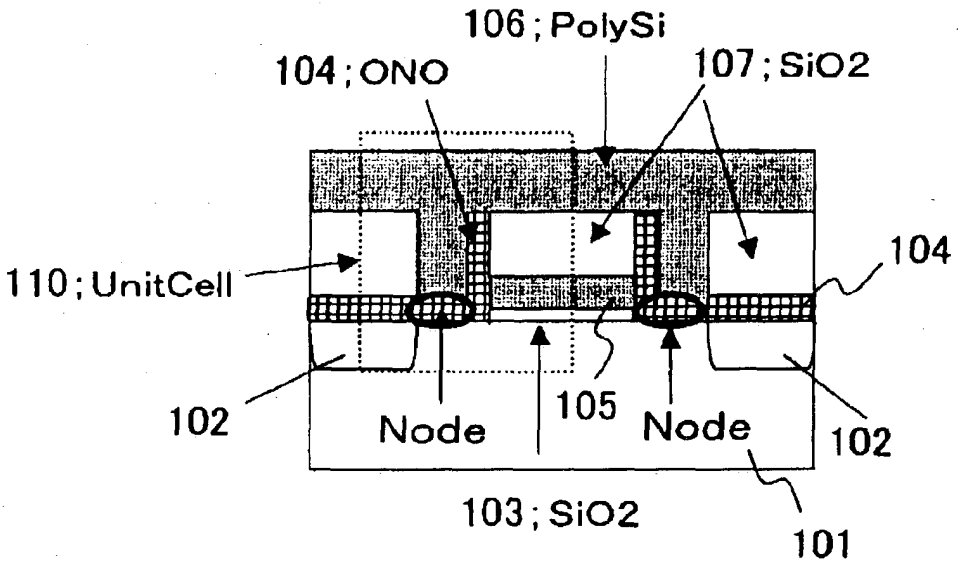

106 ; PolySi
104 ; ONO
107 ; SiO2
110 ; UnitCell
104
102
Node
105
Node
102
103 ; SiO2
101

FIG . 2

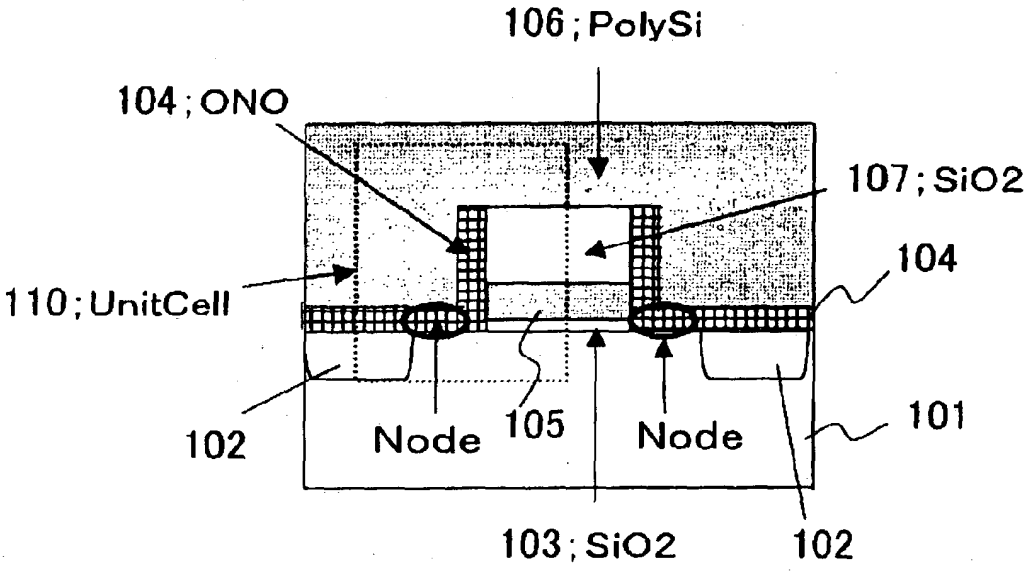

106 ; PolySi
104 ; ONO
107 ; SiO2
104
110 ; UnitCell
102
Node
105
Node
101
103 ; SiO2
102

FIG . 3A

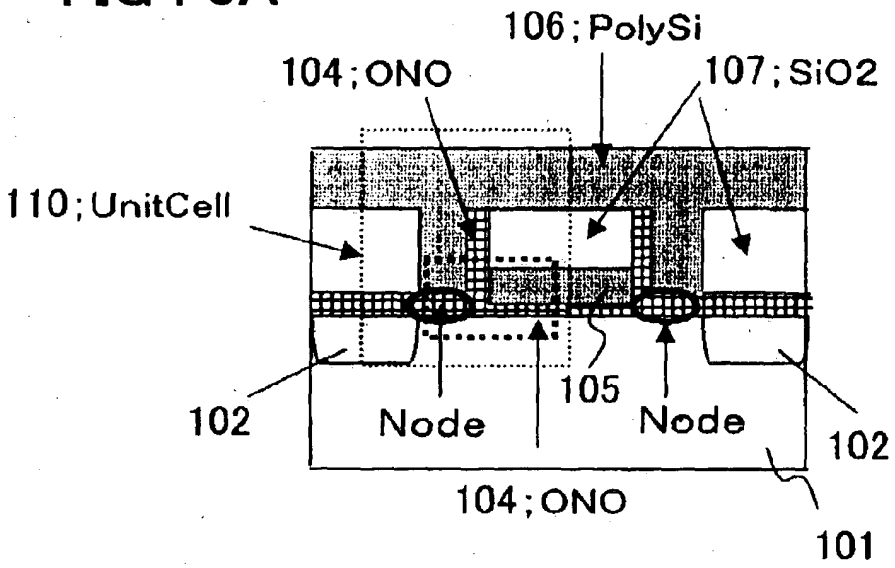
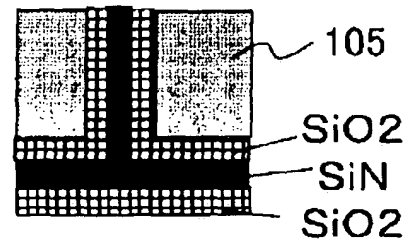


FIG . 3B



ONO STRUCTURE

FIG . 4

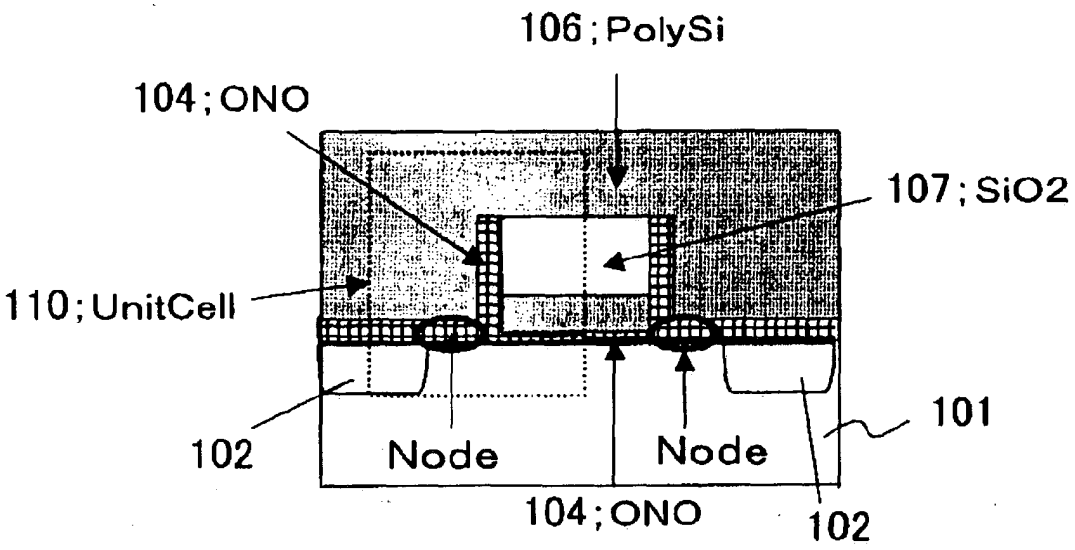

106 ; PolySi
104 ; ONO
107 ; SiO2
110 ; UnitCell
102
Node
Node
101
104 ; ONO
102

FIG . 5A

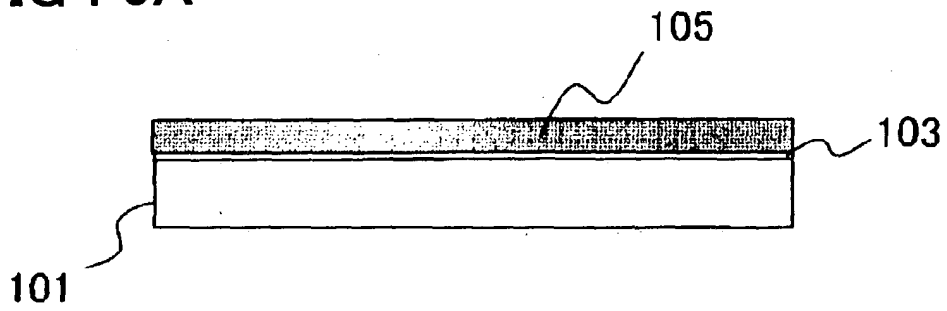


FIG . 5B

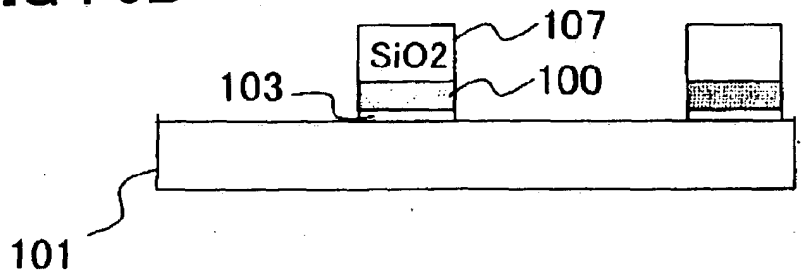


FIG . 5C

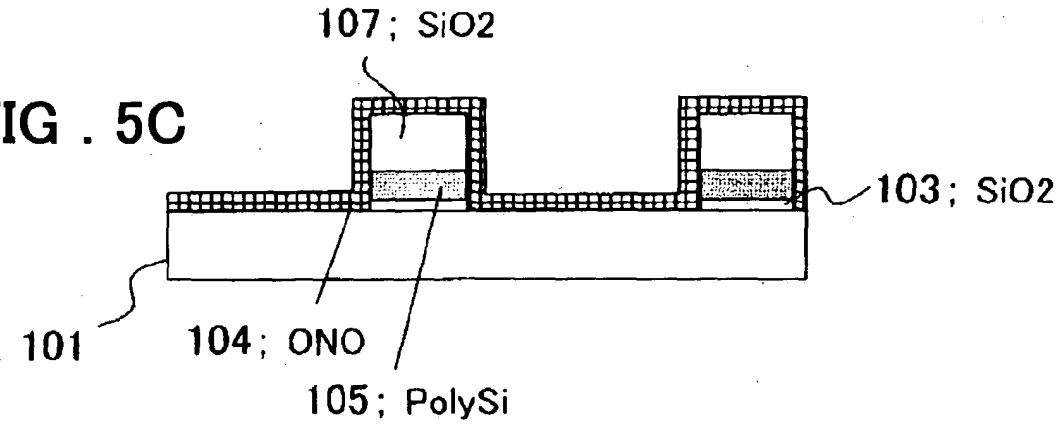


FIG . 6A

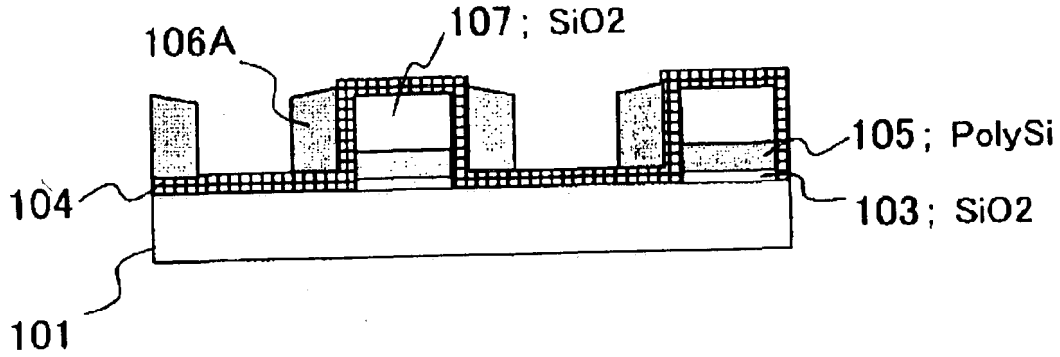

106A
107 ; SiO2
105 ; PolySi
104
103 ; SiO2
101

FIG . 6B

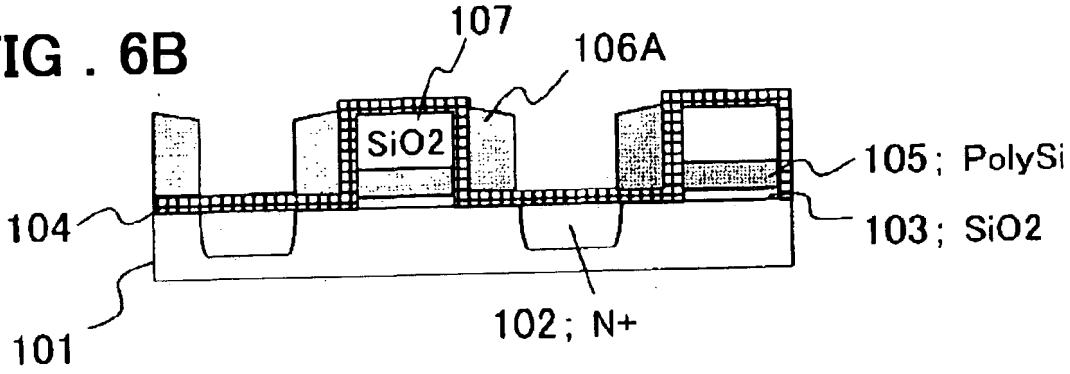

107
106A
SiO2
105 ; PolySi
104
103 ; SiO2
102 ; N+
101

FIG . 7A

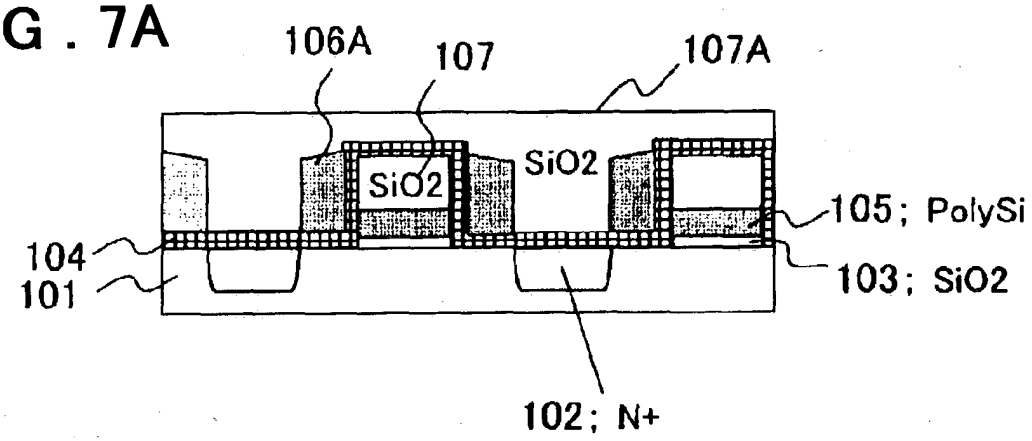

106A
107
107A
SiO2
SiO2
105; PolySi
104
101
103; SiO2
102; N+

FIG . 7B

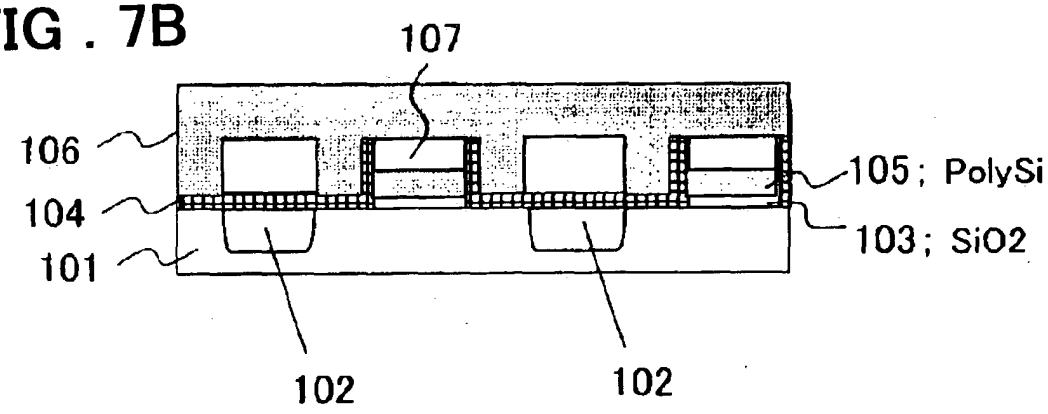

107
106
104
101
105; PolySi
103; SiO2
102
102

FIG. 8

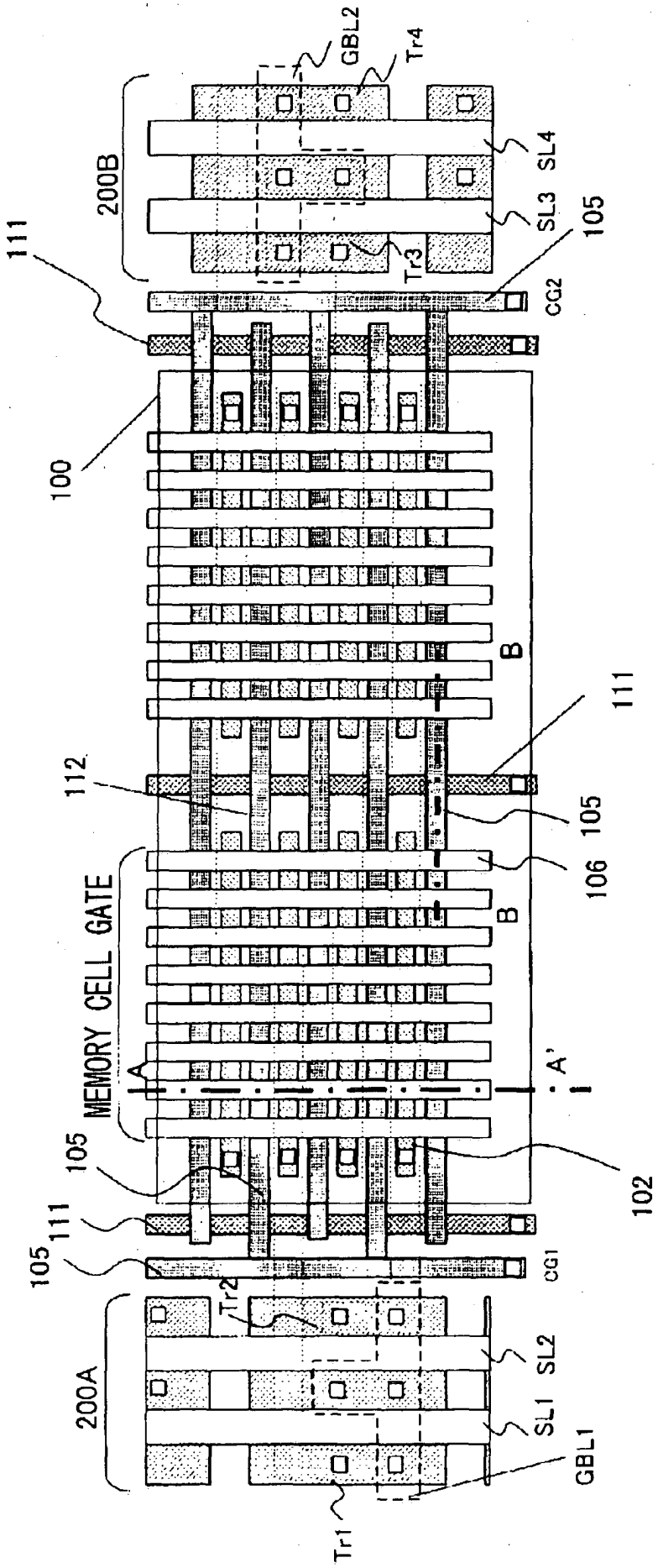

GBL2
Tr4
200B
SL4
SL3
105
111
Tr3
CG2
100
B
111
112
105
106
B
MEMORY CELL GATE
A
A'
105
102
111
105
CG1
Tr2
200A
SL2
SL1
GBL1
Tr1

FIG . 9A

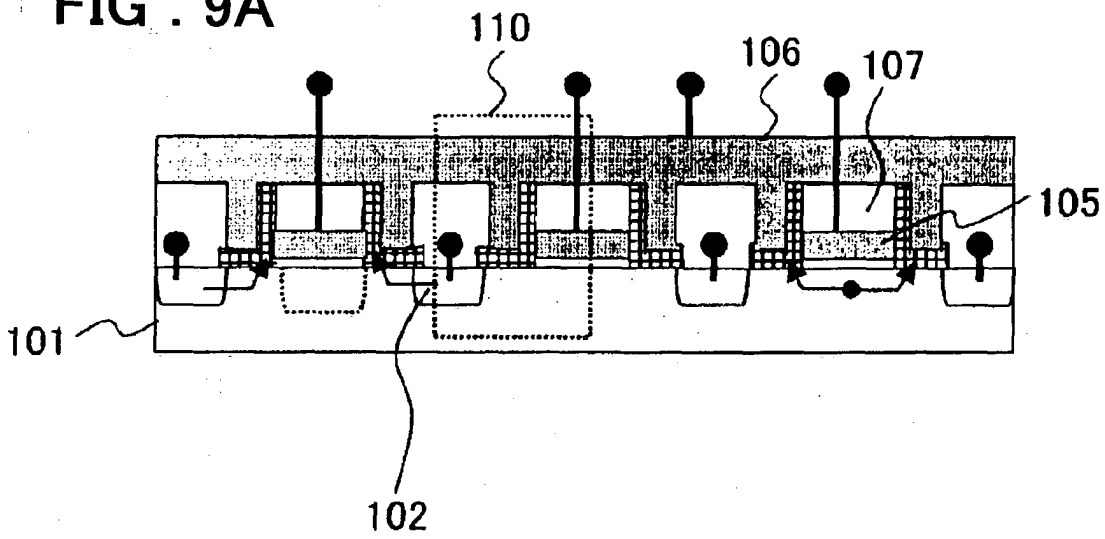


FIG . 9B

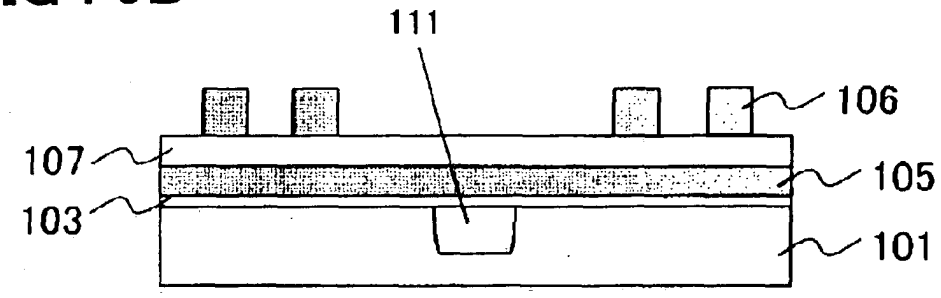


FIG. 10

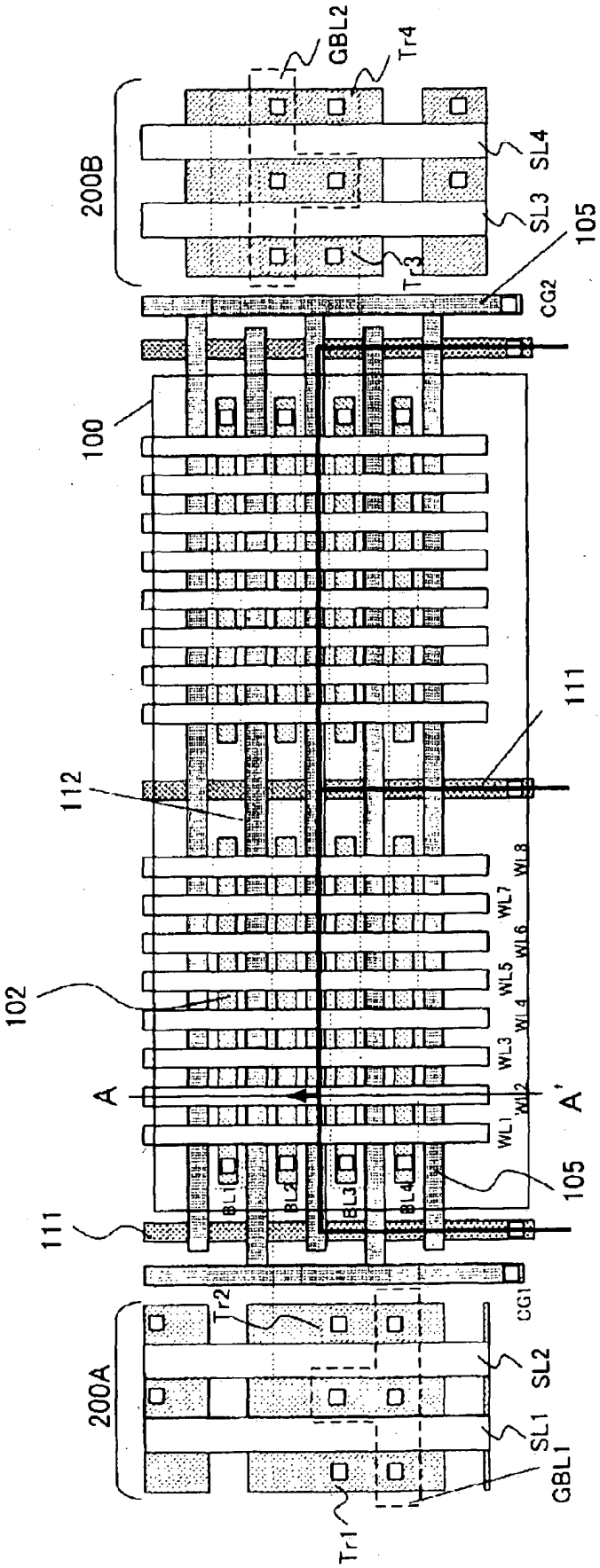

GBL2
Tr4
200B
SL4
SL3
105
Tr3
CG2
100
111
112
102
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
A
A'
105
BL1
BL2
BL3
BL4
111
CG1
Tr2
200A
SL2
SL1
GBL1
Tr1

FIG. 11

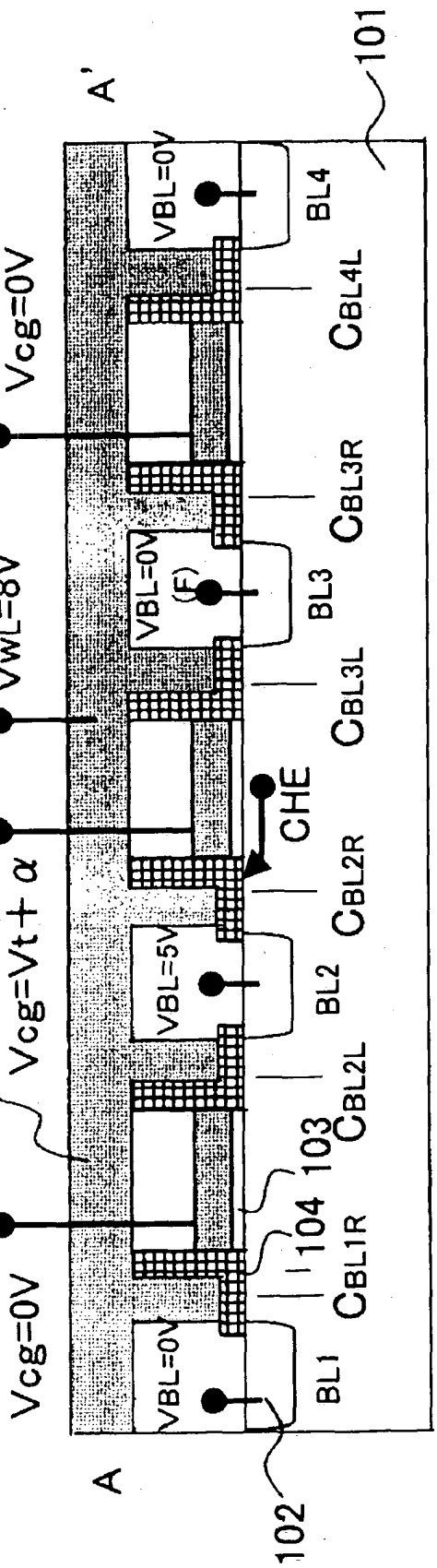

A
A'
101
102
103
104
107
Vcg=0V
Vcg=Vt+α
VWL=8V
Vcg=0V
VBL=0V
VBL=5V
VBL=0V
VBL=0V
(F)
CHE
BL1
BL2
BL3
BL4
CBL1R
CBL2L
CBL2R
CBL3L
CBL3R
CBL4L

FIG. 12

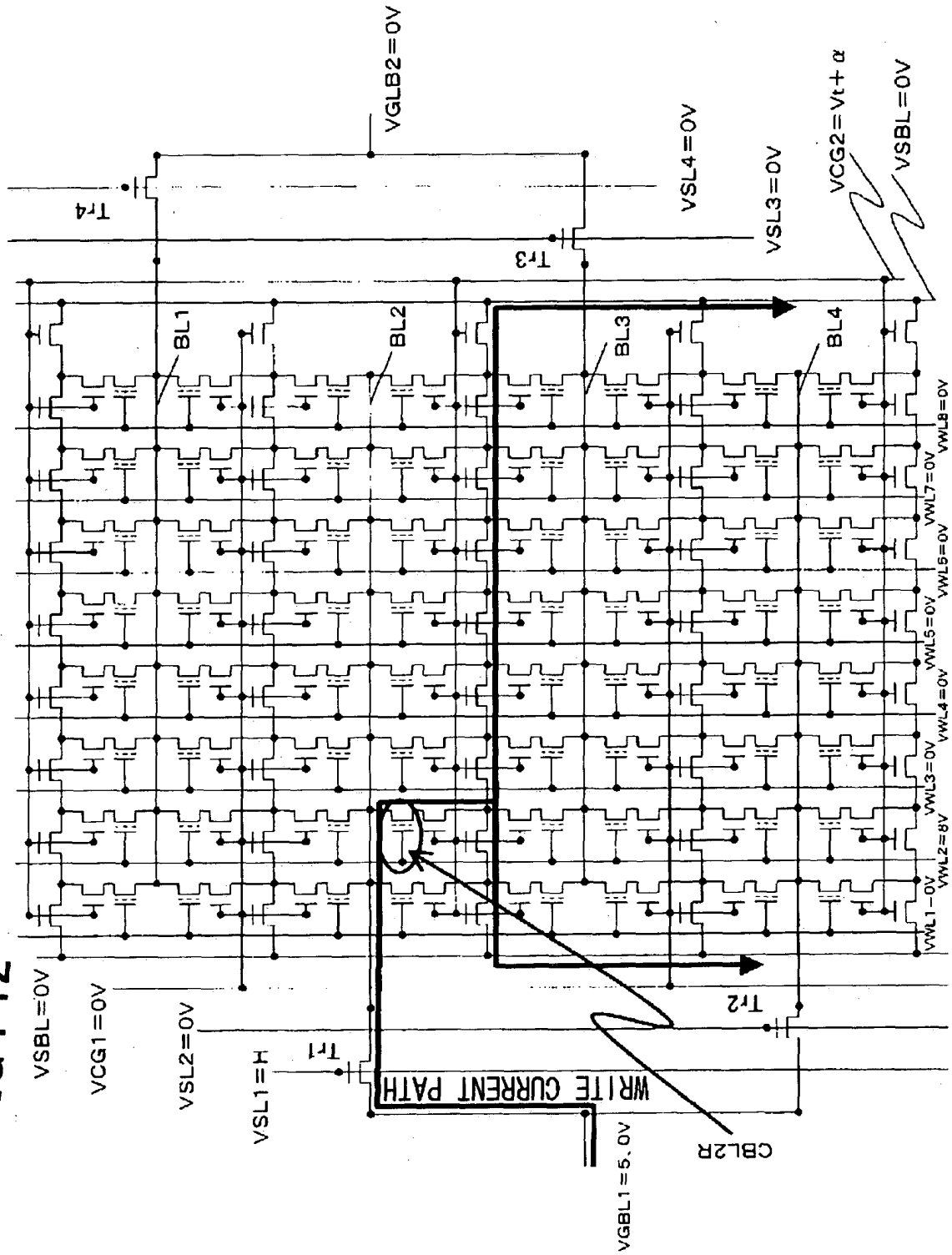
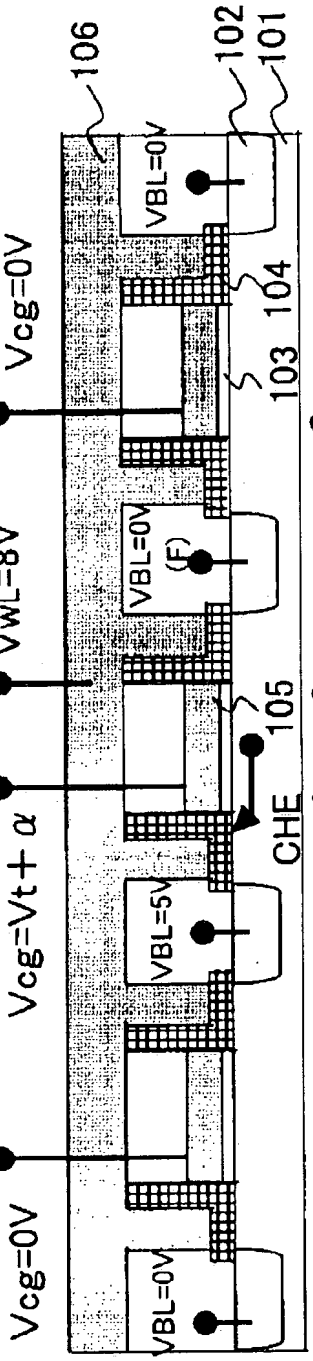
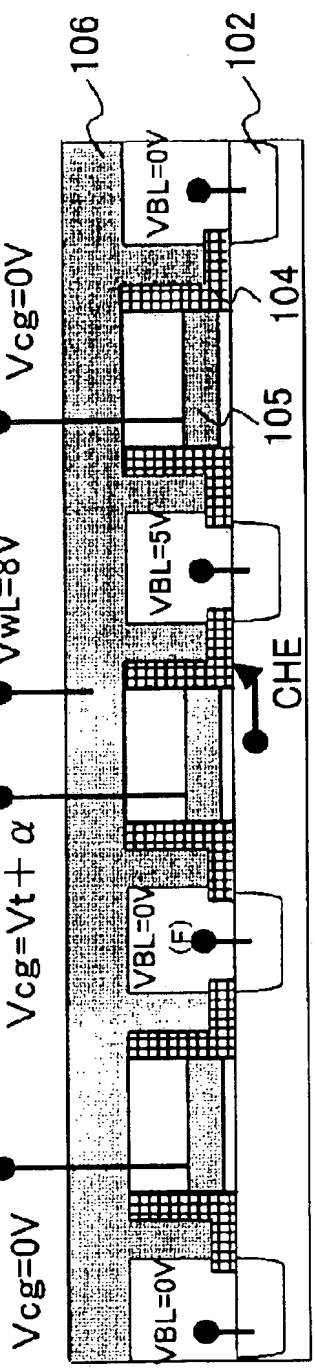

VSBL=0V
VCG1=0V
VSL2=0V
VSL1=H
Tr1
Tr2
Tr3
Tr4
VGLB2=0V
VSL4=0V
VSL3=0V
VCG2=Vt+α
VSBL=0V
BL1
BL2
BL3
BL4
WRITE CURRENT PATH
CBL2R
VGBL1=5.0V
VWL1=0V
VWL2=8V
VWL3=0V
VWL4=0V
VWL5=0V
VWL5=0V
VWL7=0V
VWL8=0V

FIG. 13A



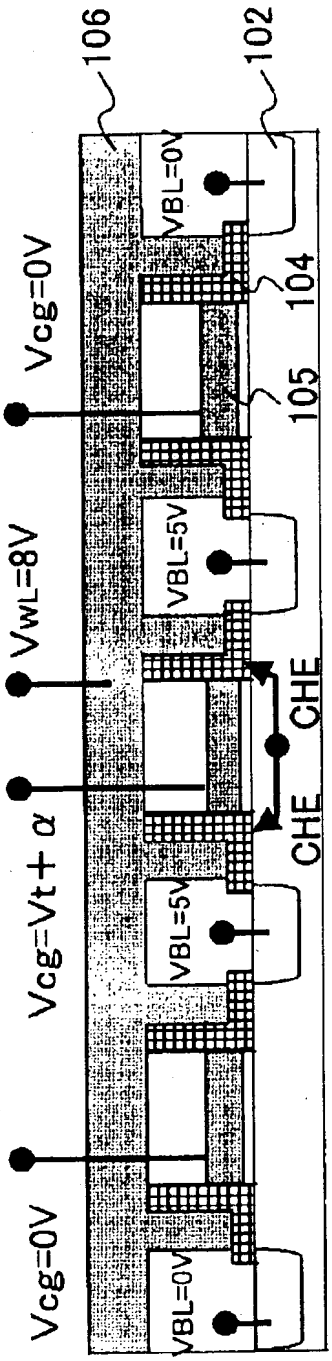
L SIDE Prog

FIG. 13B



R SIDE Prog

FIG. 13C



BOTH SIDEProg

FIG .14

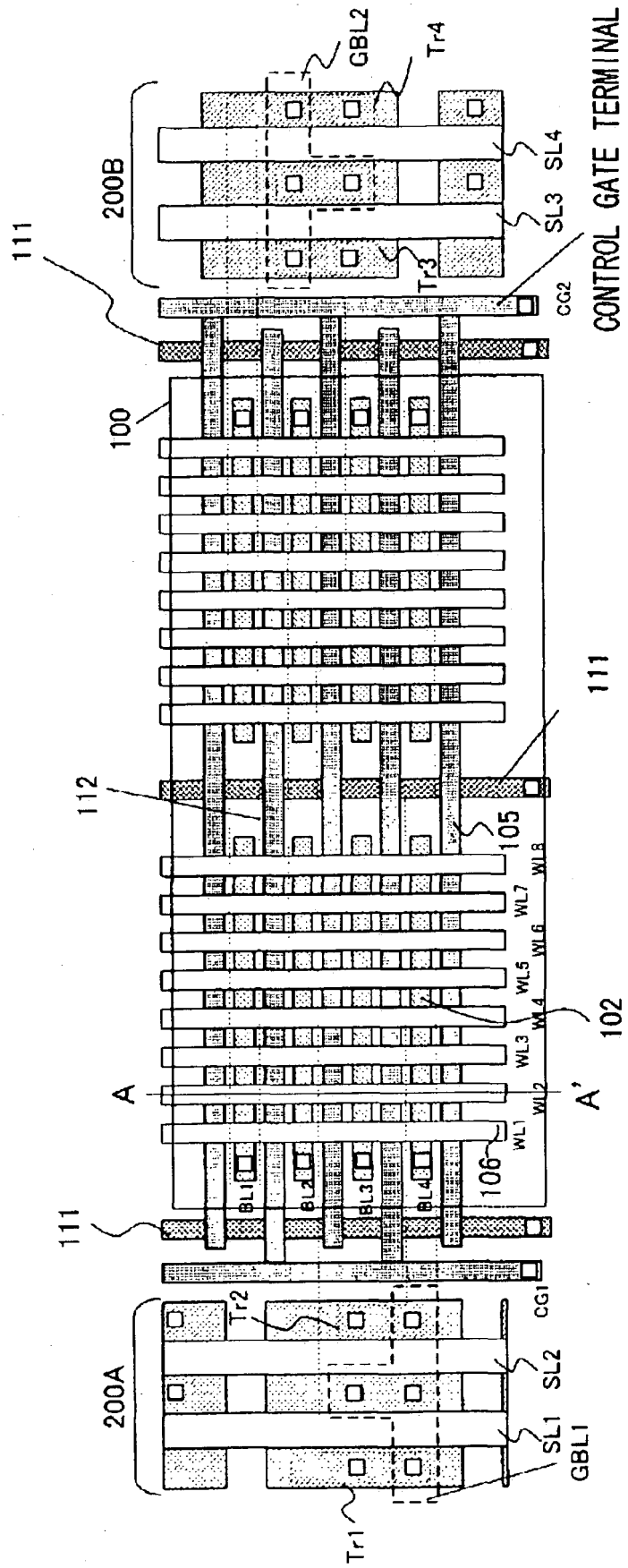

GBL2
Tr4
200B
SL4
SL3
111
Tr3
CG2
CONTROL GATE TERMINAL
100
111
112
105
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
102
A
A'
106
BL1
BL2
BL3
BL4
111
CG1
Tr2
200A
SL2
SL1
GBL1
Tr1

FIG .15

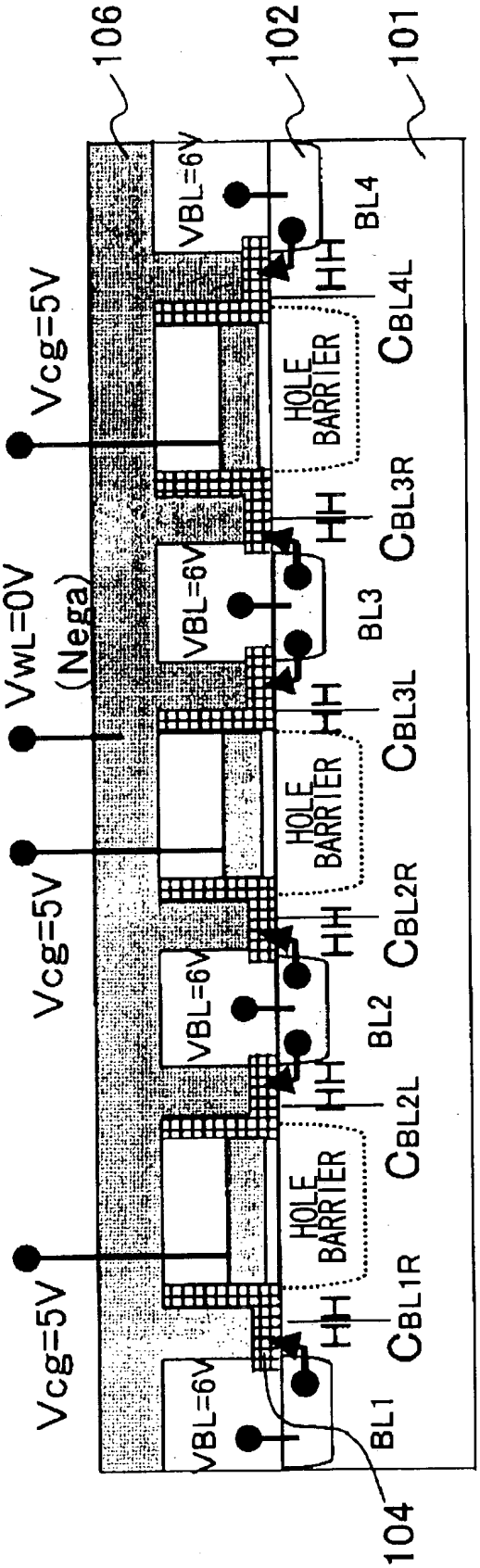

106
102
101
Vcg=5V
VWL=0V
(Nega)
Vcg=5V
Vcg=5V
VBL=6V
VBL=6V
VBL=6V
VBL=6V
HOLE BARRIER
HOLE BARRIER
HOLE BARRIER
CBL4L
CBL3R
CBL3L
CBL2R
CBL2L
CBL1R
BL4
BL3
BL2
BL1
104

FIG. 16

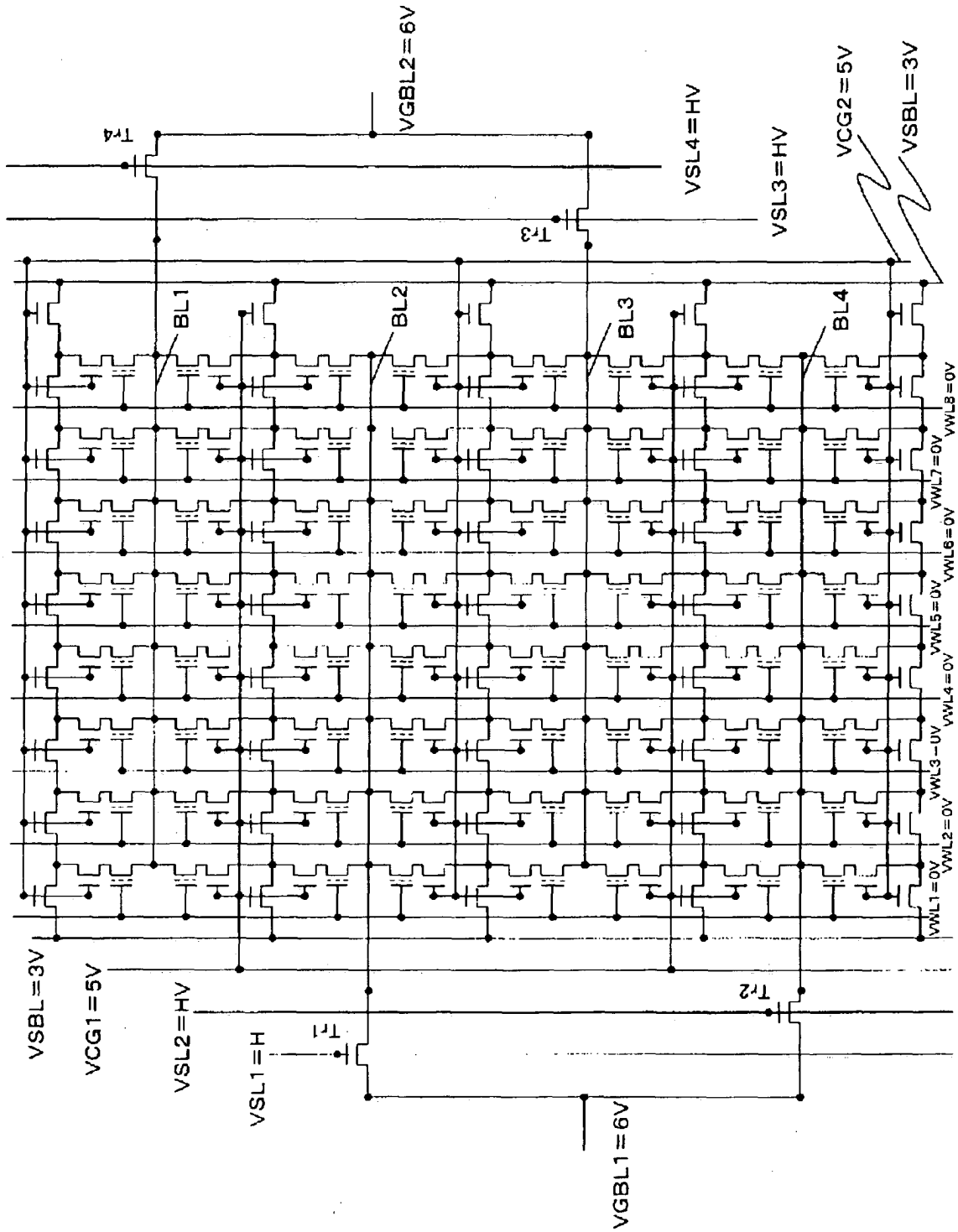

VGBL2=6V
VSL4=HV
VSL3=HV
VCG2=5V
VSBL=3V
Tr4
Tr3
BL1
BL2
BL3
BL4
VWL8=0V
VWL7=0V
VWL6=0V
VWL5=0V
VWL4=0V
VWL3=0V
VWL2=0V
VWL1=0V
VSBL=3V
VCG1=5V
VSL2=HV
VSL1=H
Tr1
Tr2
VGBL1=6V

FIG . 17A

After Prog

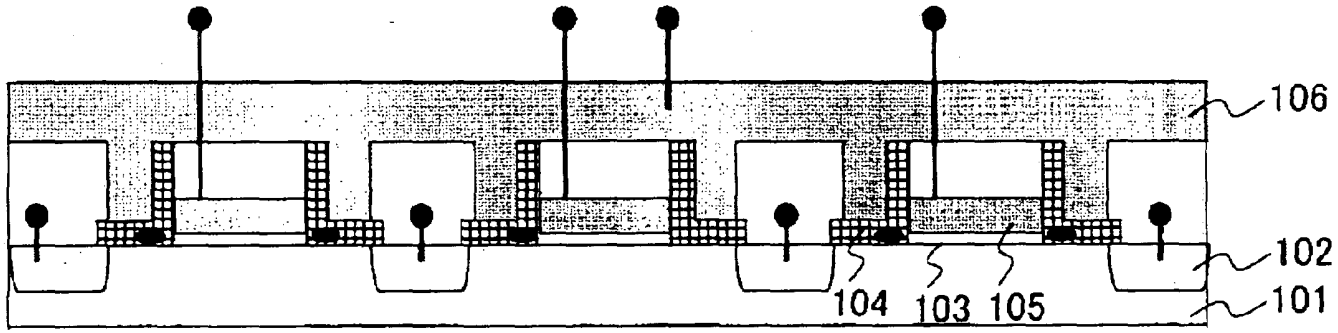


FIG . 17B

Pre Prog

Lsid ／Rside
INDEPENDENT Program

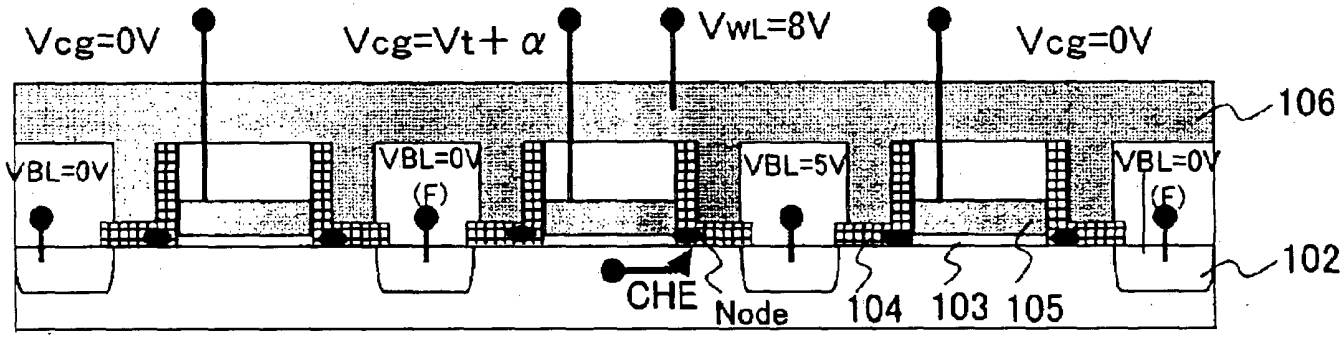


FIG . 17C

Erase

FLASH ERASE

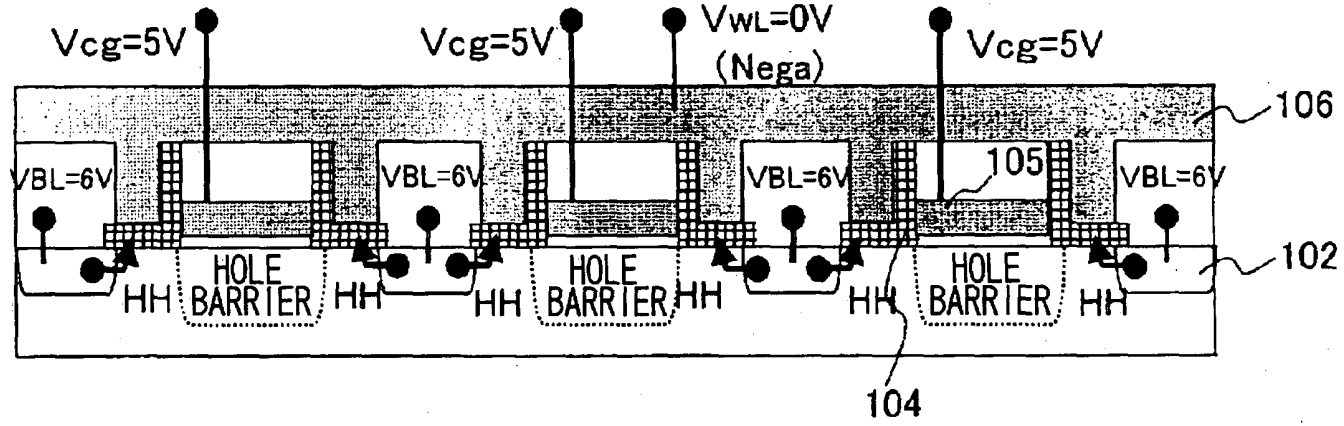


FIG. 18

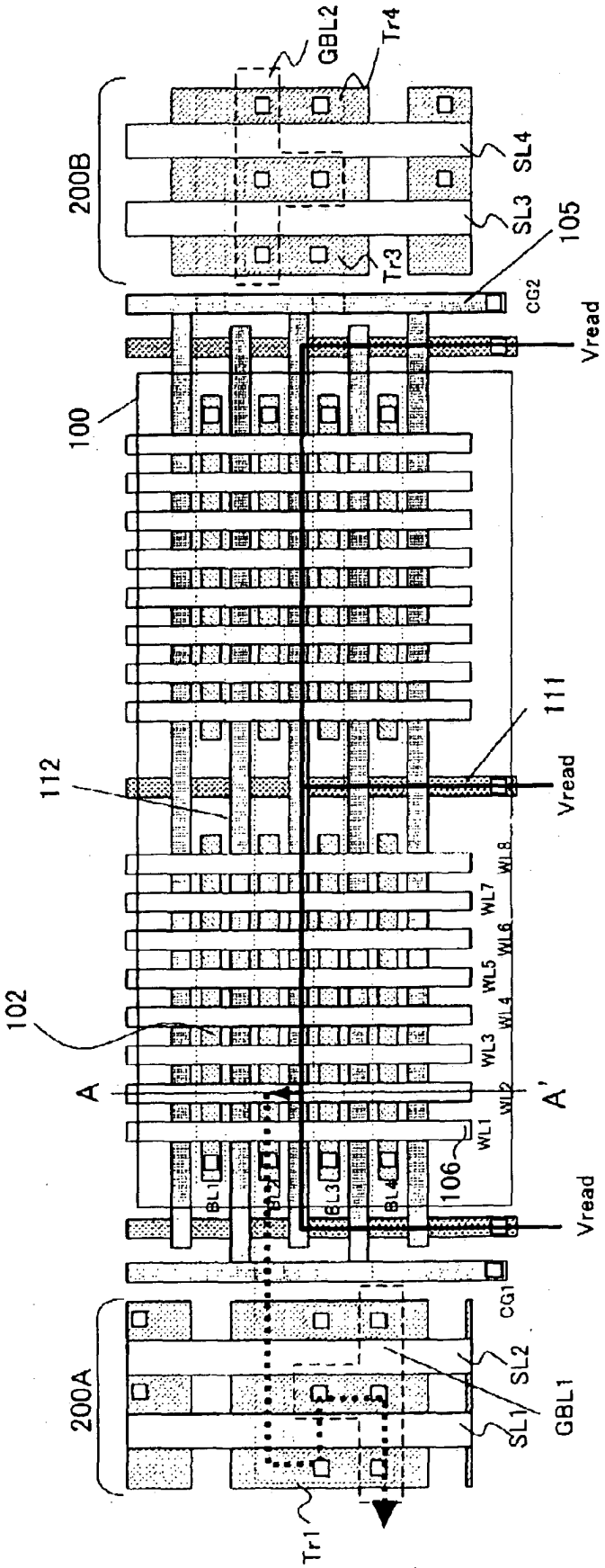

GBL2
Tr4
200B
SL4
SL3
105
Tr3
CG2
Vread
100
111
112
Vread
102
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
A
A'
106
BL1
BL2
BL3
BL4
Vread
CG1
200A
SL2
SL1
GBL1
Tr1

FIG. 19

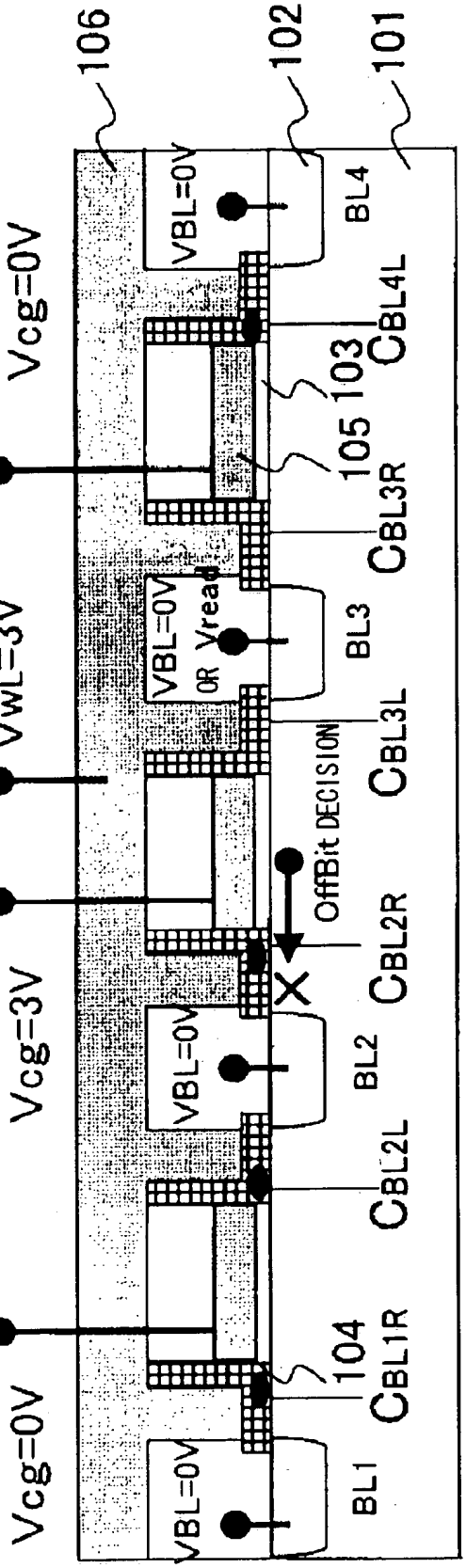

106
102
101
Vcg=0V
VBL=0V
BL4
CBL4L
103
105
CBL3R
Vcg=3V
VWL=3V
VBL=0V
OR Vread
BL3
CBL3L
OffBit DECISION
CBL2R
VBL=0V
BL2
CBL2L
104
CBL1R
Vcg=0V
VBL=0V
BL1

FIG. 20

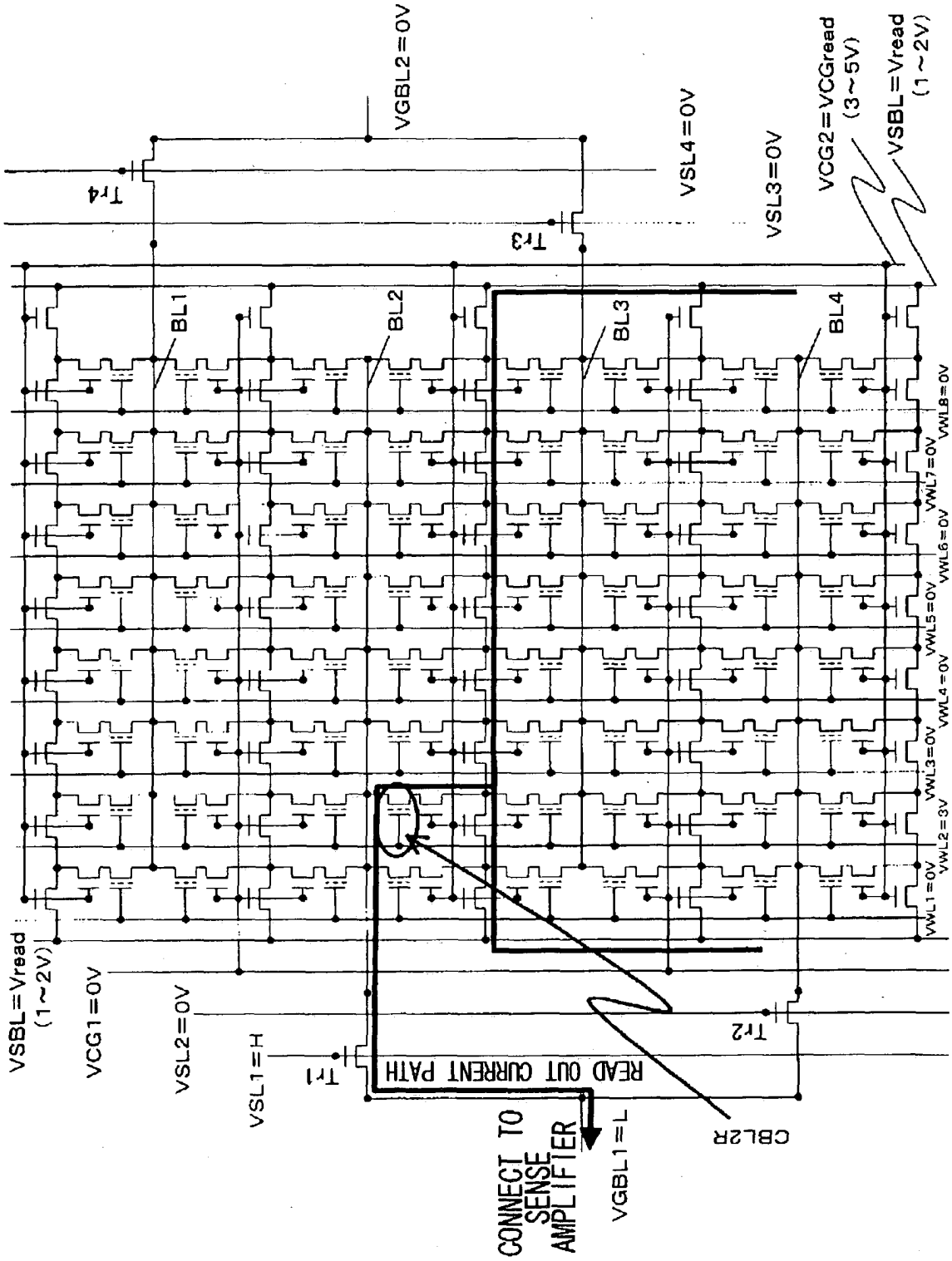

VSBL=Vread
(1~2V)
VCG1=0V
VSL2=0V
VSL1=H
Tr1
Tr2
Tr3
Tr4
VGBL2=0V
VSL4=0V
VSL3=0V
VCG2=VCGread
(3~5V)
VSBL=Vread
(1~2V)
BL1
BL2
BL3
BL4
VWL1=0V
VWL2=3V
VWL3=0V
VWL4=0V
VWL5=0V
VWL6=0V
VWL7=0V
VWL8=0V
READ OUT CURRENT PATH
CBL2R
VGBL1=L
CONNECT TO
SENSE
AMPLIFIER

FIG. 21A

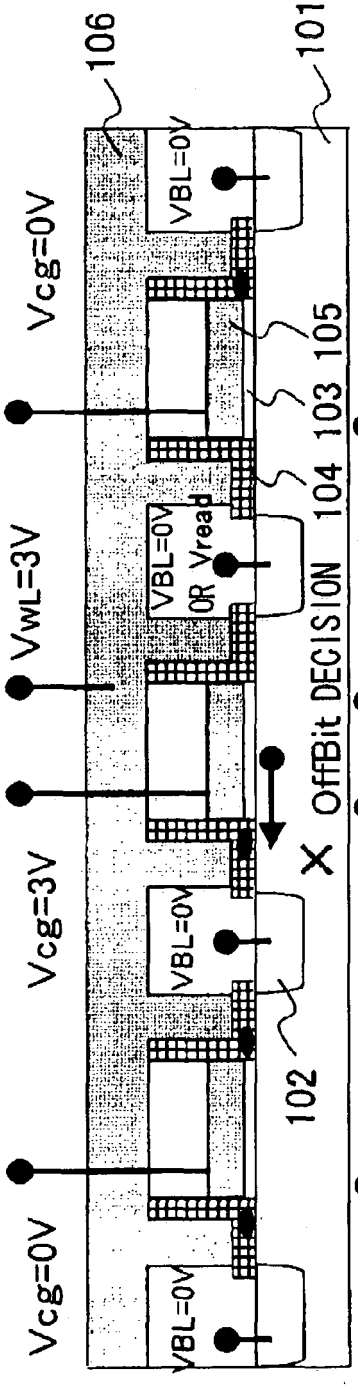


FIG. 21B

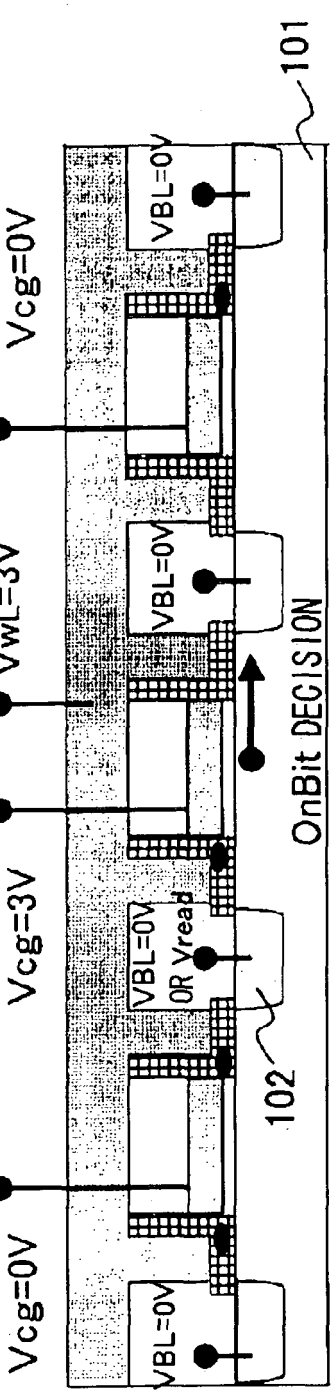


FIG. 21C

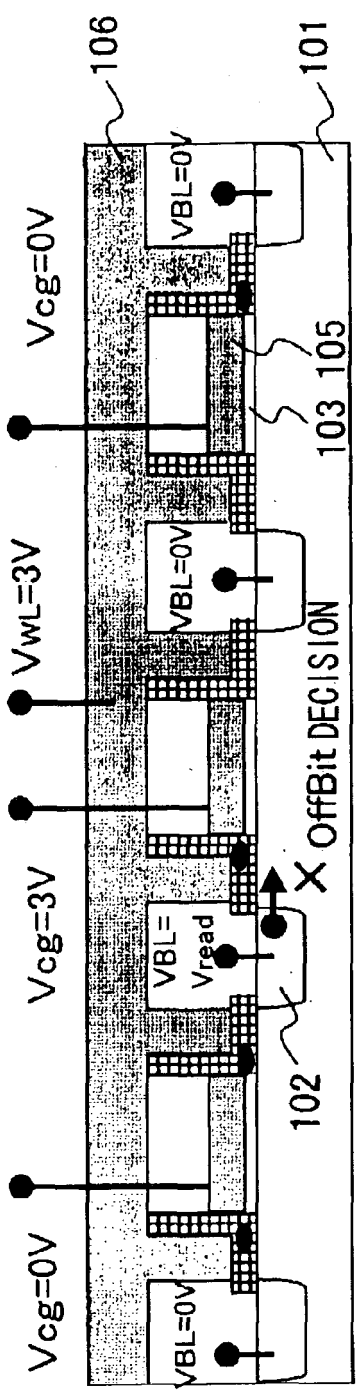


FIG . 22

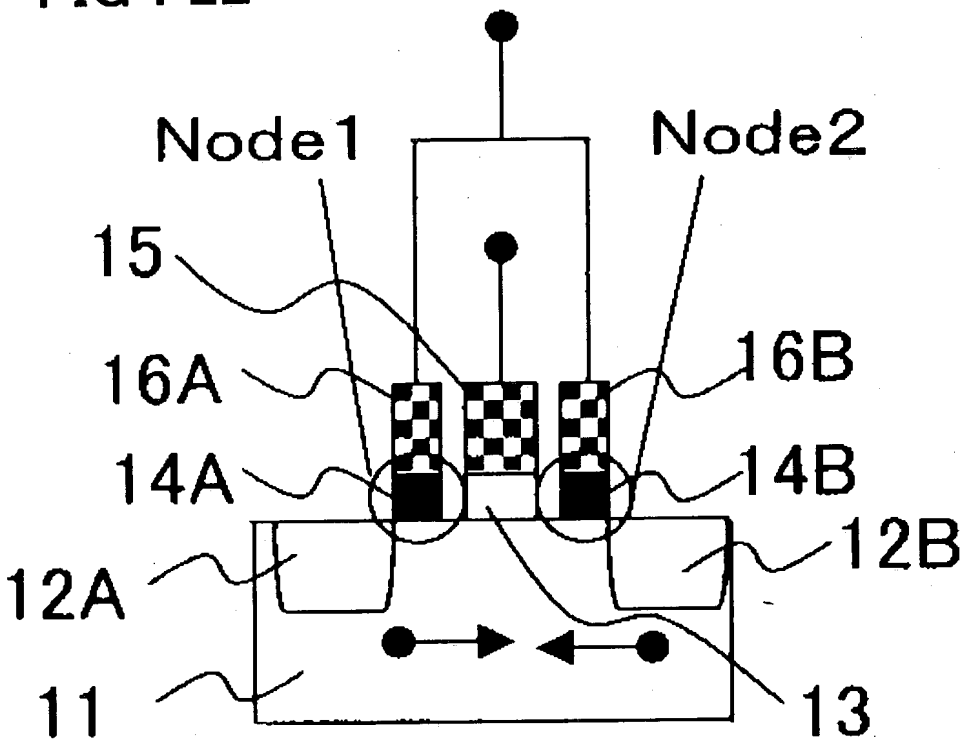


FIG . 23 PRIOR ART

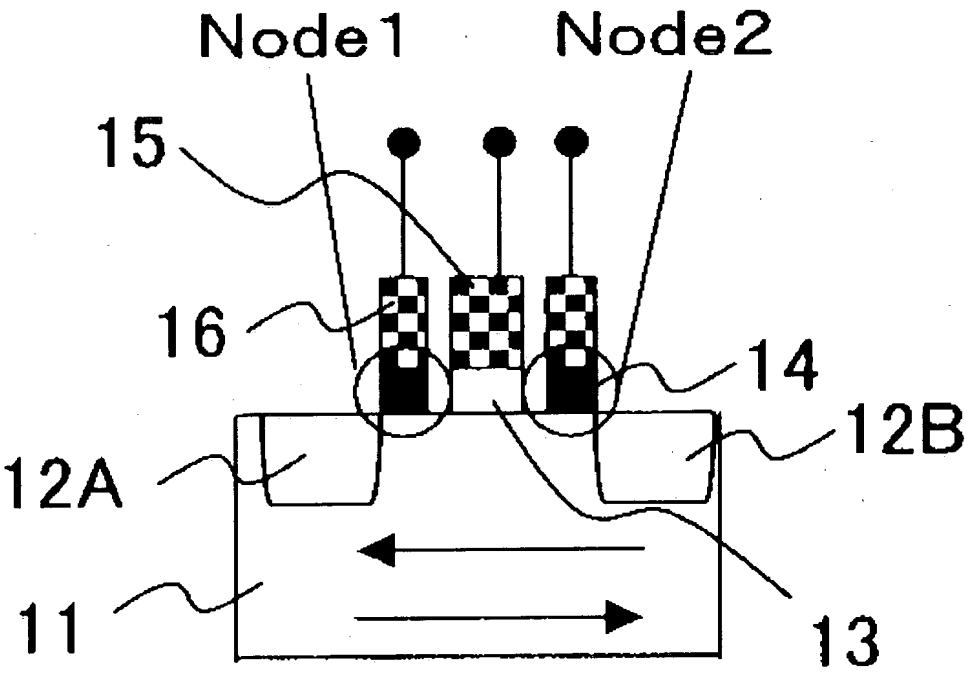


FIG . 24 PRIOR ART

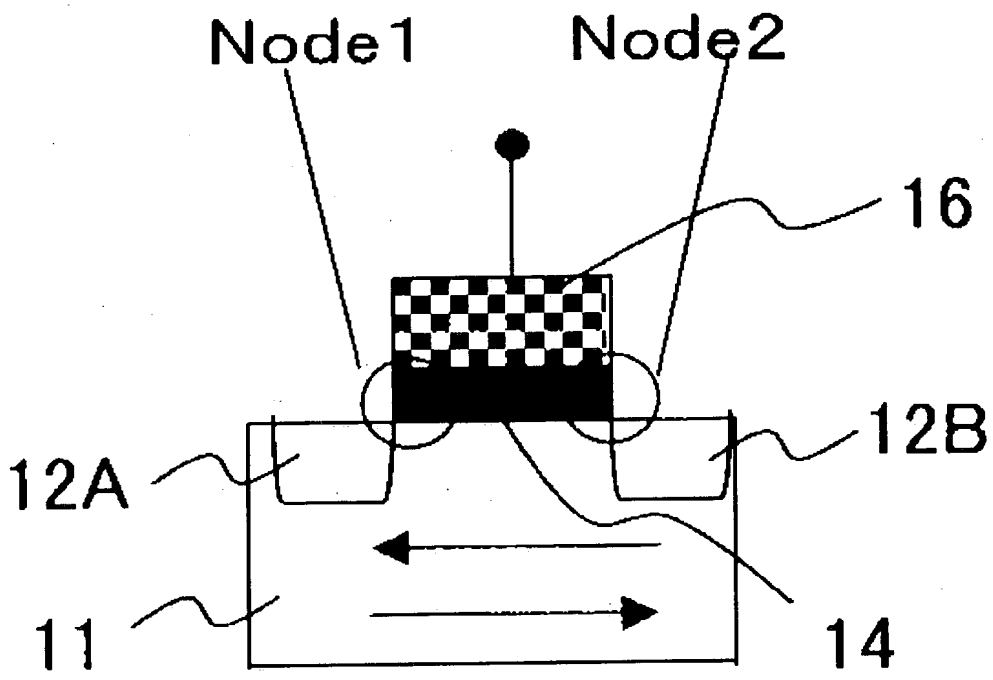


FIG . 25A PRIOR ART

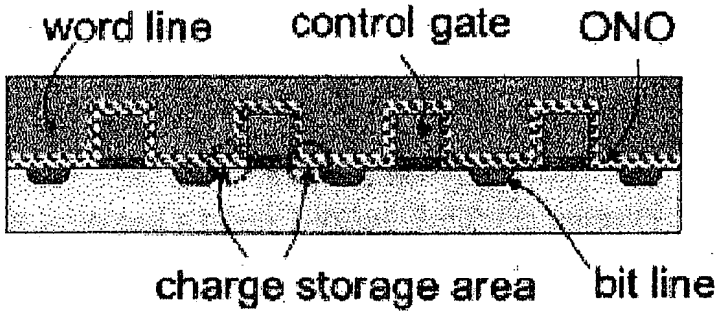


FIG . 25B PRIOR ART

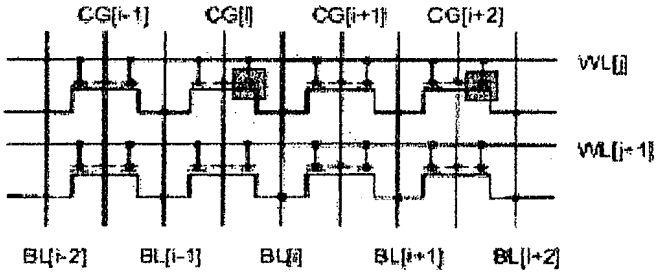


FIG . 25C PRIOR ART

	Wli (j)	WL(k≠j)	BL(I+2n)	BL(I+2n-1)	CG(I+2n)	CG(I+2n-1)
Prog	9.0V	0.0V	5.0V	0.0V	1.0V/0.0V	0.0V
Erase	0.0V	0.0V	7.0V	0.0V	5.0V	0.0V
Read	Vread	0.0V	0.0V	1.5V	1.5V	0.0V

FIG . 26A

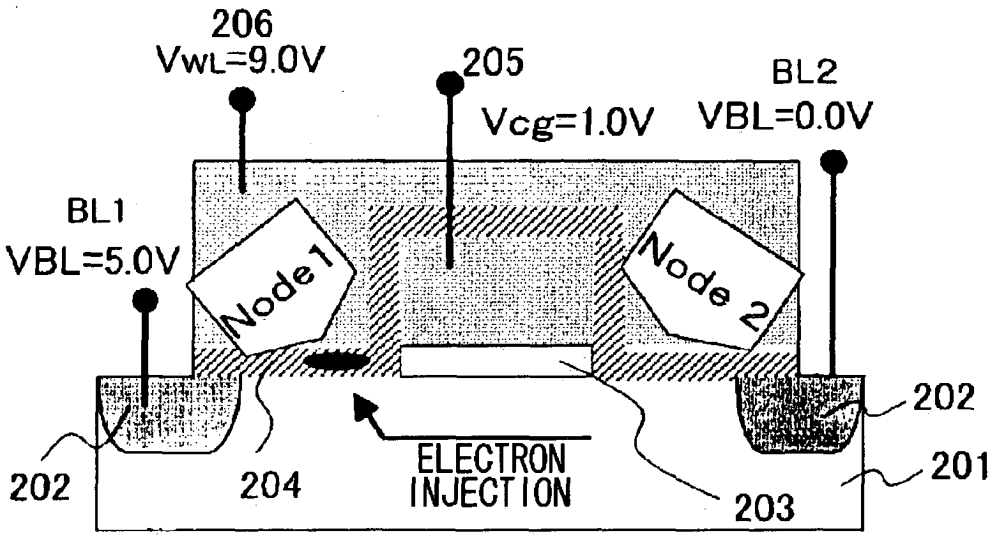


FIG . 26B

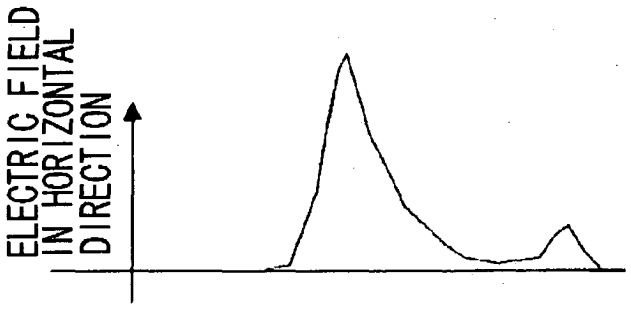


FIG . 27

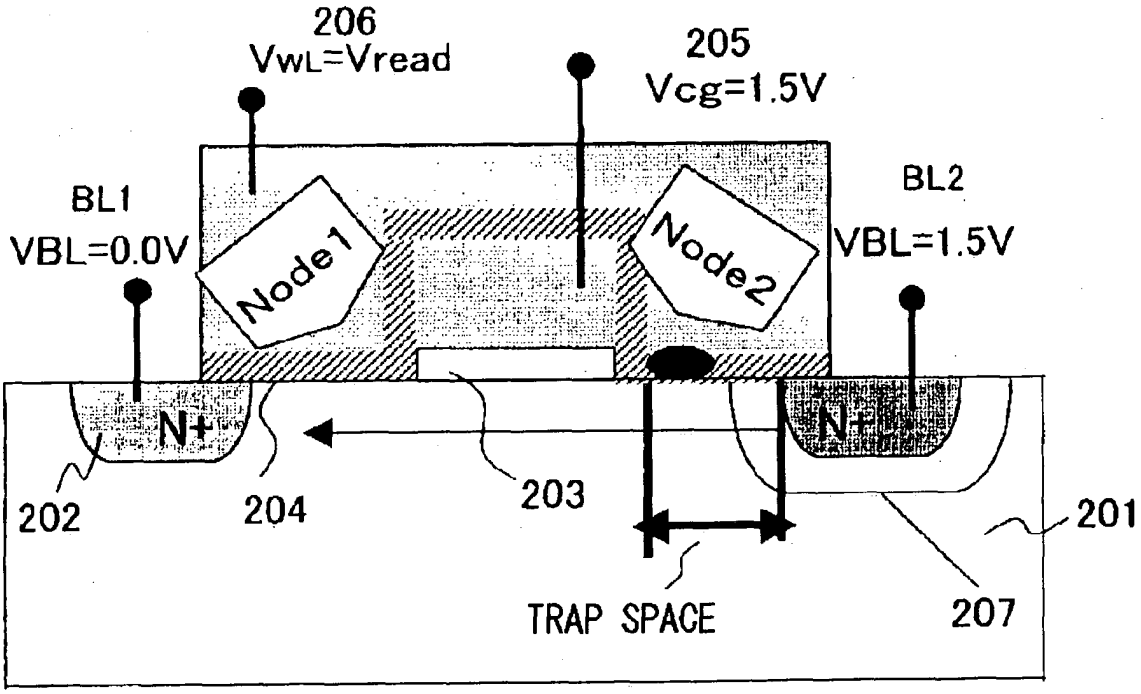
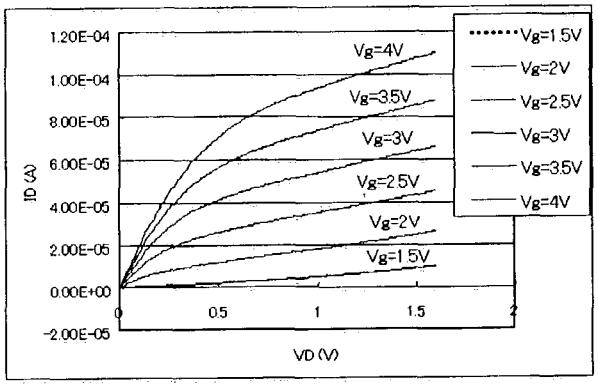
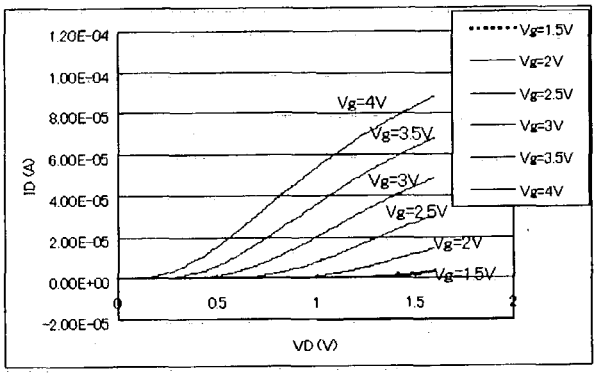

206
VwL=Vread
205
Vcg=1.5V
BL1
VBL=0.0V
BL2
VBL=1.5V
Node1
Node2
N+
N+
202
204
203
201
TRAP SPACE
207

FIG . 28A



Node1:Erased
Node2:Erased

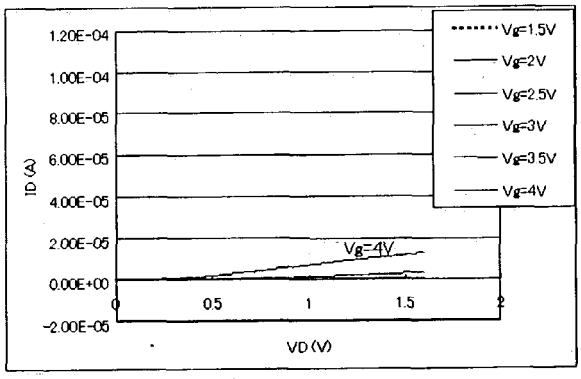
FIG . 28B



Node1:Erased
Node2:Programmed

TRAP SPACE
0.03～0.05um

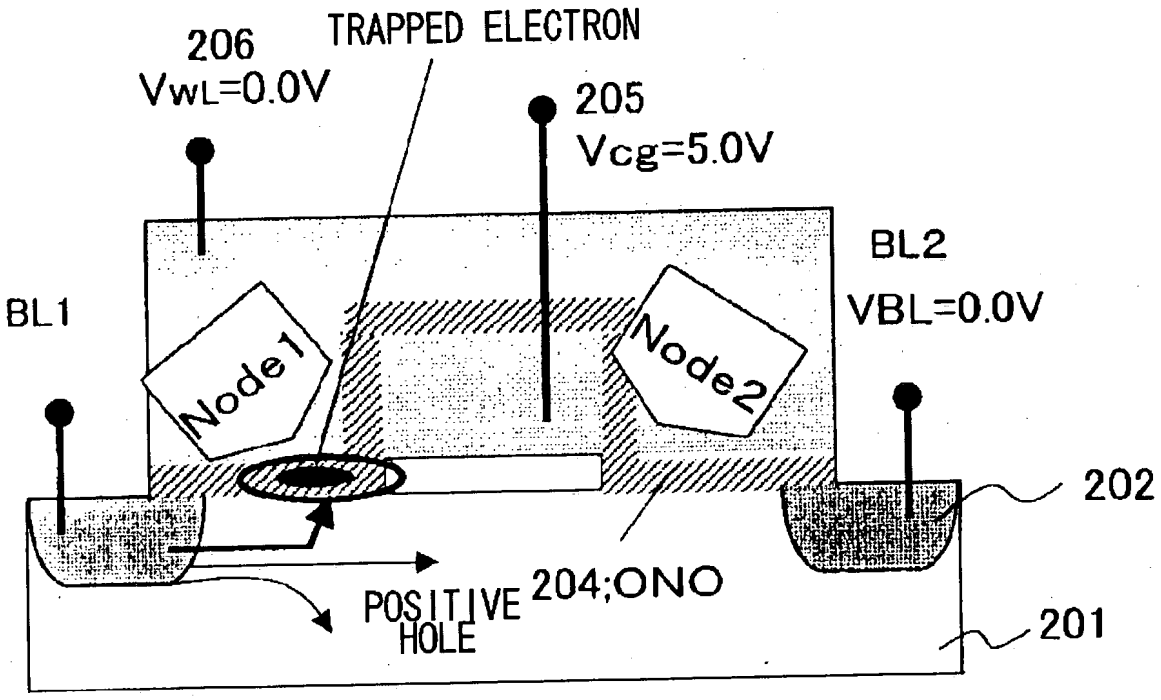
FIG . 28C



Node1:Erased
Node2:Programmed

TRAP SPACE
0.2～0.25um

FIG . 29


206
VWL=0.0V
TRAPPED ELECTRON
205
Vcg=5.0V
BL2
VBL=0.0V
BL1
Node1
Node2
202
204;ONO
POSITIVE HOLE
201